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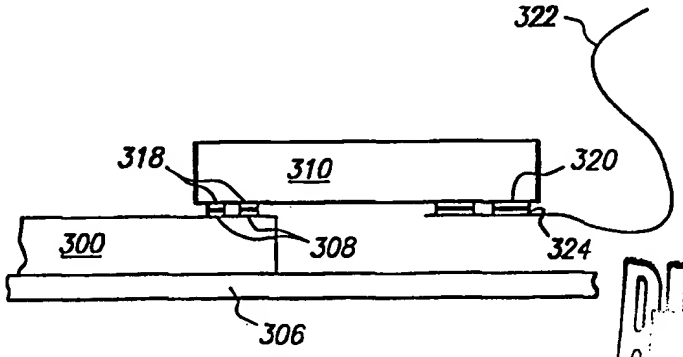
(54) Title: ELECTRICAL INTERFACE TO INTEGRATED DEVICE HAVING HIGH DENSITY I/O COUNT



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(57) Abstract

A method of and an apparatus for electrically interconnecting two integrated circuits devices includes mounting the two devices face to face. A first device is mounted for example to a substrate or lead frame. The first device includes a plurality of electrical/physical mounting structures preferably positioned along one edge. The mounting structure provides both electrical interconnection and physical mounting. A second device includes a corresponding plurality of mounting structures configured as a mirror image of the mounting structures on the first device. The mounting structures on the second device are also positioned along one of its edges so that once the mounting structures are brought together in a face to face relationship, the second device cantilevers off the edge of the first device. Under certain circumstances, a dummy block can be mounted to the substrate adjacent to the first device to act as a strut or support for the second device. The mounting structures can be positioned sufficiently close to one another that surface area consumed for I/O is minimized. Another set of electrical interconnect structures can be formed on the surface of the second device on the edge opposite the mounting structures. Electrical connection can be formed to these electrical interconnect structures using conventional techniques such as tape automated bonding.

ELECTRICAL INTERFACE TO INTEGRATED DEVICE HAVING HIGH DENSITY I/O COUNT

Field of the Invention

This invention relates to the field of forming electrical connections to integrated circuit devices. More particularly, this invention relates to forming an extremely large number of electrical connections to an integrated circuit using an inverted interface integrated circuit.

Background of the Invention

As important as manufacturing an integrated circuit is the ability to apply electronic signals to and receive electronic signals from the integrated circuit. Ordinarily, an integrated circuit die is configured to have relatively large exposed metal areas, known as bonding pads, through which this electrical interface can be conducted. Often these metal areas are formed of aluminum or an aluminum alloy can be for example 5 mils, square.

Several well known techniques are commercially used to realize such electrical interface. One such well known technique is conventionally called wire bonding. The completed die is mounted to a lead frame which is integral to the package, such as a dual-in-line package (DIP), pin grid array package (PGA), or other packages equally well known. The package includes individual pins or other electrical contact devices that are configured for ready coupling to an external circuit or circuit board through soldering, socketing or other well known means. Electrical contact is made between the bonding pads and the lead frame by attaching a thin wire between these contacts. The wire is attached to the bonding pads and the lead frame by heating or ultrasonically welding the wire to the pads. Unfortunately, the bonding wire introduces impedance into the path of an electric signal due to its thinness and length. The bonding wire acts as an inductor. This impedance operates to add noise to the signal, thereby decreasing the overall operating efficiency of a system including bonding wires. Further, because of the physical requirements of the wire and the

assembly is made to the back of the upper integrated circuit using for example conventional wire bonding techniques.

Still others have proposed techniques for reducing the volume and thus surface area consumed by multiple integrated circuit devices. One such technique is taught in U.S. Patent 5,491,612 to Nicewarner, Jr. This technique is not concerned with the number of interconnections between integrated circuits but rather the volume of space consumed by plural integrated circuits. Nicewarner teaches a three dimensional modular assembly of integrated circuits. The chips are mounted back to back and are mounted on both sides of the primary substrate and between each of the two secondary substrates and the primary substrate. Because of the design, the array of chips between the primary substrate and the first secondary substrate must mirror the array of chips between the primary substrate and the second secondary substrate.

Yet others have proposed stacking integrated circuits one on top of another. Such techniques include forming interconnections along the sides of the stack. Heat dissipation from an integrated circuit within the stack can become a problem.

An emerging technology surrounds semiconductor micromachines that are used for forming displays. A device that can be used for such a display is disclosed in U.S. Patent 5,311,360 which is incorporated in its entirety herein by reference.

According to the teachings of the '360 patent, a diffraction grating is formed of a multiple mirrored-ribbon structure such as shown in Figure 1. A pattern of a plurality of deformable ribbon structures 100 are formed in a spaced relationship over a substrate 102. Both the ribbons and the substrate between the ribbons are coated with a light reflective material 104 such as an aluminum film. The height difference that is designed between the surface of the reflective material 104 on the ribbons 100 and those on the substrate 102 is $\lambda/2$ when the ribbons are in a relaxed, up state. If light at a wavelength λ impinges on this structure perpendicularly to the surface of the substrate 102, the reflected light from the surface of the ribbons 100 will be in phase with the reflected light from the substrate 102. This is because the light which strikes the substrate travels $\lambda/2$ further than the light striking

would be extremely complex. This would tend to further reduce the yield of such a structure and thereby further increase the cost. For these reasons, it is preferred that the drive electronics be placed in a separate integrated circuit.

Interconnections to such a device could not require the electrically conductive vias nor the bridging technique taught by Rostoker. Further, such an interconnecting structure could not function using a stacked arrangement because light would not be able to impinge onto the surface of the active display area.

What is needed is a method of and apparatus for providing electrical interconnections directly from one integrated circuit to another.

What is also needed is a method of and an apparatus for providing electrical interconnections to an integrated circuit with extremely high°I/O requirements.

What is further needed is a method of and an apparatus for providing electrical interconnections to an integrated circuit without obscuring the surface of the integrated circuit.

Summary of the Invention

A method of and an apparatus for electrically interconnecting two integrated circuits devices includes mounting the two devices face to face. A first device is mounted for example to a substrate or lead frame. The first device includes a plurality of electrical/physical mounting structures preferably positioned along one edge. The mounting structure provide both electrical interconnection and physical mounting. A second device includes a corresponding plurality of mounting structures configured as a mirror image of the mounting structures on the first device. The mounting structures on the second device are also positioned along one of its edges so that once the mounting structures are brought together in a face to face relationship, the second device cantilevers off the edge of the first device. Under certain circumstances, a dummy block can be mounted to the substrate adjacent to the first device to act as a strut or support for the second device. Under certain other circumstances, an epoxy potting compound can be used to provide structural support.

form such as a printed circuit board, a ceramic or an IC package. A plurality of electrical/physical mounting structures 308 are formed near one edge on the primary surface 302 of the semiconductor device 300. The mounting structures 308 are preferably formed of a metal using conventional semiconductor processing techniques. The mounting structures 308 are electrically coupled to the integrated circuit (not shown) using conductive traces (either metallic or doped semiconductor). The mounting structure 308 can be conveniently formed of aluminum or an aluminum alloy. Other metals can also be used.

A second semiconductor device 310 is substantially planar and includes a primary face 312 and a secondary face 314. An integrated circuit device (not shown) is formed in the primary face 312 of the second semiconductor device 300. The integrated circuit formed on the second semiconductor device 300 can be of any type of circuit but is preferably of a driver circuit for a semiconductor micromachine display device. However, it will be apparent to one of ordinary skill in the art that the second integrated circuit device 310 could be another conventional circuit such as a microprocessor, controller, PAL, PLA, dynamic or non-volatile memory and the like.

The primary surface 312 of the second semiconductor device 310 is mounted to the primary surface 302 of the first semiconductor device 300 as shown by the dash-dot-dash line. As can be readily seen the second semiconductor device 310 cantilevers off the edge of the first semiconductor device 300 in an overhanging manner. This limits the amount of the primary surface 302 of the first semiconductor device 300 that is consumed with forming electrical connections to the integrated circuit on the semiconductor device 300. Because of the techniques described herein, the size of the mounting structure 308 can be as small as 50 microns on a side. The spacing between adjacent mounting structure 308 can be limited to 50 microns.

A plurality of electrical/physical mounting structures 318 are formed near one edge on the primary surface 312 of the semiconductor device 310. The mounting structures 318 and portions of the second semiconductor device 310 along with their respective lead lines are shown as ghost lines to indicate that those structures are hidden from view. The

The process for forming the structure of Figures 3 and 4 follows. Separately, the first and the second semiconductor devices 300 and 310 are formed using semiconductor processing steps known and described in detail elsewhere. Either the mounting structures 308 or the mounting structures 318 or both include a mounting substance such as solder. Once completed, the first semiconductor device 300 is mounted to the substrate 306. Separately, a flexible tape connector 322 is mounted to the second semiconductor device 310. Once these two subassemblies are formed, the second semiconductor device 310 with the flexible tape connector 322 are brought to the first semiconductor device 300. The mounting substance is melted with heat or ultrasonically to join the mounting structures 308 and 318 electrically and physically.

Under certain circumstances, it may be determined that the strength of the joined mounting structures 308 and 318 will be insufficient to hold the second semiconductor device 310 in place without failing. Under those circumstances a support structure 330 is used as shown in Figure 5. The support structure 330 is mounted adjacent the edge of the first semiconductor device 300 to which the second semiconductor device 310 is mounted. The support structure 330 can be formed of a dummy block of semiconductor material or can be formed of a defective/non-functioning device such as the first semiconductor device 300. It is desirable that the height of the support structure 330 approximate that of the first semiconductor device 300. An adhesive material 332 is placed on an upper surface of the support structure 330 to hold the second semiconductor device 310 in place. Preferably, the adhesive 332 is formed of a compressible material so that it will conform to an ideal height for supporting the second semiconductor device 310.

As an alternative to the structure shown in Figure 5, where it is determined that the strength of the joined mounting structures 308 and 318 will be insufficient to hold the second semiconductor device 310 in place without failing a potting compound 340 can be used as shown in Figure 6. According to the preferred embodiment of such a compound, an epoxy potting compound is used. Under those circumstances a support structure 330 is used as shown in Figure 5. The support structure 330 is mounted adjacent the edge of the first

CLAIMS

What is claimed is:

1. A method of electrically and structurally coupling two integrated circuits together comprising the steps of:

a. providing a first substantially planar semiconductor substrate having a first face and a second face, having a first integrated circuit formed in the first face and having a plurality of first integrated circuit electrical contacts positioned along a first edge of the first face;

b. providing a second substantially planar semiconductor substrate having a third face and a fourth face, having a second integrated circuit formed in the third face and having a plurality of second integrated circuit electrical contacts positioned along a second edge of the third face, the third face having a third edge opposite the second edge; and

c. juxtaposing the first integrated circuit electrical contacts to the second integrated circuit electrical contacts in a face to face relationship such that the first substantially planar semiconductor substrate overlaps the second substantially planar substrate only in a region of the first and second integrated circuit electrical contacts but is not substantially overlapping otherwise such that the second edge is substantially unsupported.

2. The method according to claim 1 wherein the first integrated circuit comprises a pixel structure of a micromachine display device and wherein the second integrated circuit comprises a driver circuit formed on the third face for coupling to and controlling the first integrated circuit.

10. An electrical system comprising:

a. a first substantially planar substrate having a first primary surface, having a first integrated circuit formed in the first primary surface, and having a secondary surface opposite to the first primary surface, wherein a first plurality of integrated circuit electrical contacts are positioned along a first edge of the first primary surface;

b. a second substantially planar substrate having a second primary surface, and having a second integrated circuit formed in the second primary surface, the second primary surface having a third edge opposite a second edge, wherein a second plurality of integrated circuit electrical contacts are positioned along the second edge of the second primary surface; and

c. an electrical interface for juxtaposing the first plurality of integrated circuit electrical contacts in a face to face relationship with the second plurality of integrated circuit electrical contacts such that the first substantially planar substrate overlaps the second substantially planar substrate only in a region of the first and second integrated circuit electrical contacts but is not substantially overlapping otherwise such that the third edge is substantially unsupported.

11. The electrical system according to claim 10 wherein the first integrated circuit comprises a multiple mirrored-ribbon structure and wherein the second integrated circuit comprises a driver circuit for coupling to and controlling the first integrated circuit.

12. The electrical system according to claim 10 further comprising a third substantially planar substrate wherein the first secondary surface is mounted to the third substantially planar substrate.

13. The electrical system according to claim 10 further comprising a third plurality of integrated circuit electrical contacts positioned along the third edge for coupling to a flexible tape structure.

17. The cantilevered flip-chip assembly according to claim 16 further comprising a third plurality of integrated circuit electrical contacts positioned along the third edge of the second substantially planar substrate for coupling to a flexible tape structure and for making external connections to other integrated circuits.

18. The cantilevered flip-chip assembly according to claim 16 further comprising a non-electrical support structure coupled to and mounted underneath the second substantially planar substrate for holding the second substantially planar substrate in place.

19. The cantilevered flip-chip assembly according to claim 19 wherein the non-electrical support structure is formed of a block of semiconductor material.

20. The cantilevered flip-chip assembly according to claim 19 wherein the non-electrical support structure is formed of a potting compound.

21. The cantilevered flip-chip assembly according to claim 20 wherein the potting compound is an epoxy potting compound.

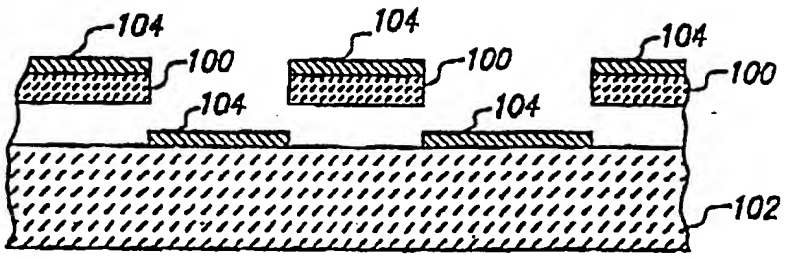

FIG. 1 (PRIOR ART)

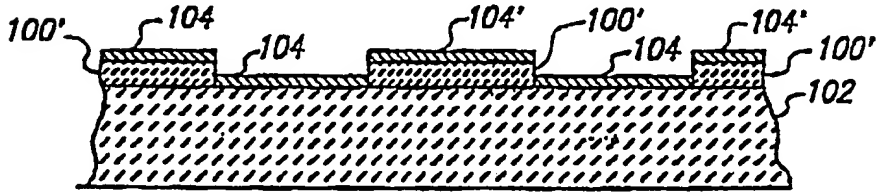

FIG. 2 (PRIOR ART)

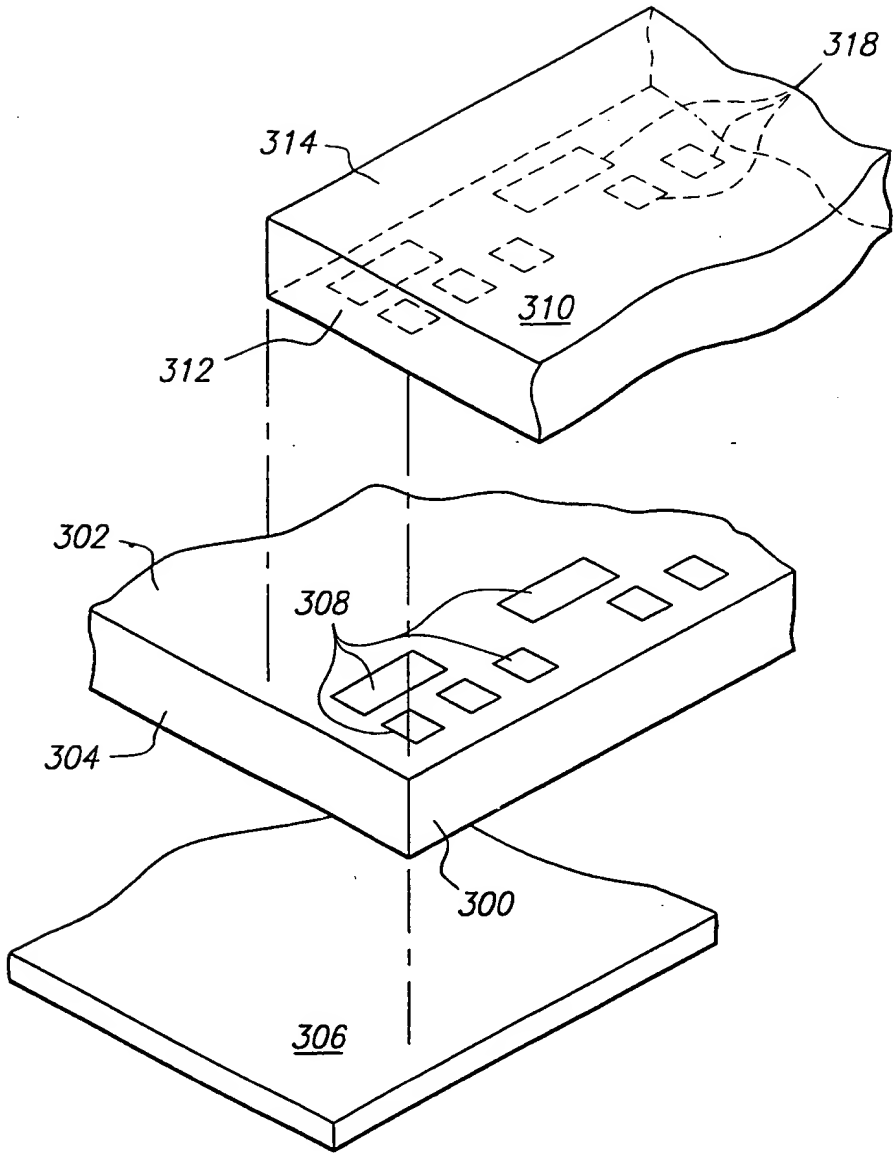

FIG. 3

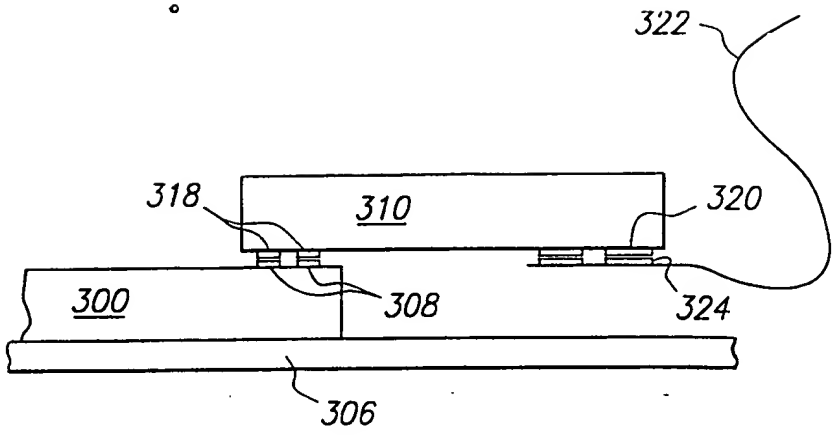
322
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FIG. 4

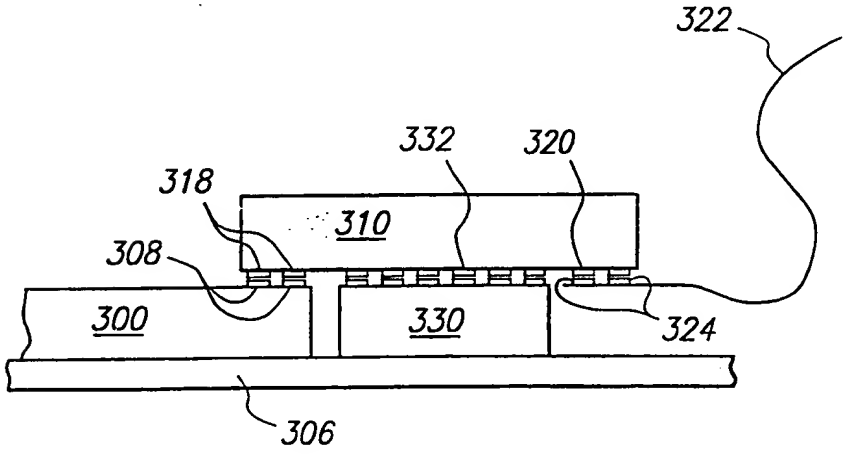
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FIG. 5

INTERNATIONAL SEARCH REPORT

Inter. nal Application No
PCT/US 98/13220

A. CLASSIFICATION OF SUBJECT MATTER
IPC 6 H01L25/065

According to International Patent Classification (IPC) or to both national classification and IPC

B. FIELDS SEARCHED

Minimum documentation searched (classification system followed by classification symbols)
IPC 6 H01L

Documentation searched other than minimum documentation to the extent that such documents are included in the fields searched

Electronic data base consulted during the international search (name of data base and, where practical, search terms used)

C. DOCUMENTS CONSIDERED TO BE RELEVANT

Category *	Citation of document, with indication, where appropriate, of the relevant passages	Relevant to claim No.
A	EP 0 304 263 A (LSI LOGIC CORP) 22 February 1989 Entire document	1,10,16
A	C.N. LIU ET AL: "Integrated Circuit Chip Package" IBMTDB, vol. 17, no. 7, 31 December 1974, page 2018 XP002076742 Entire document	1,8-10, 12,16, 20,21
A	PATENT ABSTRACTS OF JAPAN vol. 017, no. 586 (P-1633), 26 October 1993 & JP 05 173160 A (SEIKO EPSON CORP), 13 July 1993 see abstract	1-6, 10-18

-/--

[X] Further documents are listed in the continuation of box C.

[X] Patent family members are listed in annex.

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Date of the actual completion of the international search	Date of mailing of the international search report
8 September 1998	22/09/1998

Name and mailing address of the ISA	Authorized officer
European Patent Office, P.B. 5818 Patentlaan 2 NL - 2280 HV Rijswijk Tel. (+31-70) 340-2040, Tx. 31 651 epo nl, Fax: (+31-70) 340-3016	Odgers, M

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INTERNATIONAL SEARCH REPORT

Information on patent family members

Inter. ional Application No
PCT/US 98/13220

Patent document cited in search report	Publication date	Patent family member(s)	Publication date
EP 0304263 A	22-02-1989	JP 1157561 A	20-06-1989